



Information Technology Laboratory

ERDC High Performance Computing Major Shared Resource Center

Background The Engineer Research and Development Center (ERDC) High Performance Computing (HPC) Major Shared Resource Center (MSRC) is committed to enabling Department of Defense (DoD) Science and Technology and Test and Evaluation missions by providing leading-edge computational hardware and world-class computational engineering expertise and leadership to the DoD in support of the warfighter.

Expertise ERDC MSRC computing resources include 6.4 TFLOPS of computing capability: a 64-processor Cray X1; two 512-processor SGI Origin 3900s; a 512-processor SGI Origin 3800; a 1,904-processor Cray T3E (the largest such system in the world); a 512-processor Compaq SC40; a 512-processor Compaq SC45; and 500+ terabytes of robotic storage. Access to the ERDC MSRC HPC systems is provided through the Defense Research and Engineering Network (DREN) and the Internet.

The ERDC MSRC Scientific Visualization Center (SVC) provides the capability to analyze the results of complex computational simulations and models. The SVC offers state-of-the-art techniques for data interpretation to engineers and scientists, providing them with the tools, hardware, and expertise to derive insight from terabytes of data. The SVC also provides conceptual visualization capabilities to complement the traditional data visualization techniques. These capabilities take advantage of industry-leading animation and modeling software, enabling DoD scientists to communicate all aspects of their research by setting their results in context.

In addition to the staff of the SVC, the MSRC includes a Computational Science and Engineering (CS&E) group and onsite representatives from the Programming Environment and Training (PET) program. The CS&E group specializes in application performance tuning, code parallelization, performance measurement, and parallel application design for DoD applications. This team is internationally recognized, and their accomplishments include pioneering work with multilevel parallelism, developing of the ANSI (American National Standards Institute) Pthreads standard for FORTRAN, and leading the hardware performance evaluation effort for the DoD High Performance Computing Modernization Program.

The PET program at the ERDC MSRC joins leading universities and national HPC research centers with DoD researchers to identify ways to improve DoD HPC applications and computing environments. The purpose of the PET initiative is to enhance the programming environment for ERDC MSRC users through training and technology transfer from universities.

Benefits The ERDC MSRC ensures that DoD scientists and engineers across the Nation have immediate access to the best HPC hardware and expertise the industry has to offer. By utilizing DoD HPC resources, these scientists and engineers significantly cut defense system costs by shortening the design cycle and reducing reliance on expensive and destructive live experiments and prototype demonstrations.

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